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Power and Read Delay Efficient Sensor based Compensation Technique for Low Power SRAM

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***Abstract*—Due to scaling in CMOS technology, the leakage current increases and this increase in leakage current affects the operation of SRAM. Therefore techniques for reducing the leakage current are acquiring more importance. Even though a high V_{th} CMOS can be considered as a solution to the mentioned problem, it will affect the operational speed of SRAM. Therefore a new technique consisting of a leakage current sensor and a compensation circuit is proposed. The leakage current sensor is used to sense the voltage drop due to the leakage current and a compensation circuit is used to speed up the read operation of SRAM when a leakage is detected. By the measurement results, the read delay is reduced by 28% and power is reduced by 40% when compared to uncompensated SRAM.**

***Index Terms*— CMOS, compensation, leakage current, SRAM.**

I. INTRODUCTION

Static Random-Access Memory (SRAM) is fabricated using advanced processes in order to extend the operational time and to obtain a reduction in power dissipation. Advancement of technology towards the nanometer scale increases the leakage and it becomes a serious threat. As the leakage current rise exponentially with the decrease in threshold voltage (V_{th}) and gate oxides the operational frequency and the power consumption of SRAMs is degraded "Ref. [1–3]". Even though a high V_{th} CMOS can be considered as a solution to the mentioned problem, the operational speed of SRAM is affected.

The conventional six-transistor SRAM shown in Fig.1 contains two inverters which are connected back to back (M1, M2, M3and M4) and two access transistors (M5 and M6) that are connected to the bit lines (Bitline(BL) and bit line bar (BLB). The access transistors are used to provide access to internal nodes and the cross-coupled inverters are used to store the two stable states i.e. 0 and 1. Unlike DRAM, SRAM does not require any refresh operation and it will store data as long as the power is on. Conventional 6T SRAM has very low Read Noise Margin and in order to obtain it, the pull-down transistor (M2 and M4) width is increased but this increases the SRAM area thereby increasing the leakage currents. The scaling of supply voltage leads to power consumption reduction during the active operation. There are three operational modes for an SRAM and they are: standby (or hold) mode, read mode, and write mode.

In standby mode, the word line is provided with a low voltage (i.e. WL=0). The access transistors M6 and M5 are in off condition and therefore the access transistors and the bit lines remain disconnected. In this mode, the two inverters continue to provide feedback as long as supply is provided and thus the data

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continues to remain in the latch. In read mode, the bit lines are initially precharged to V_{DD} and the word line is also enabled (i.e. WL=1). The access transistors are connected to the bit lines as the word line is high and this allows transfer of values in the nodes (QB and Q) to bit lines "Ref. [5]". If the value at node Q is 1 then the bit line BLB gets discharged through the transistor M4 while the bit line BL remains at logical 1. For the write '0' operation the bit line BL is pulled down to 0V while bit line BLB is pulled high to V_{DD} and the word line is also enabled.

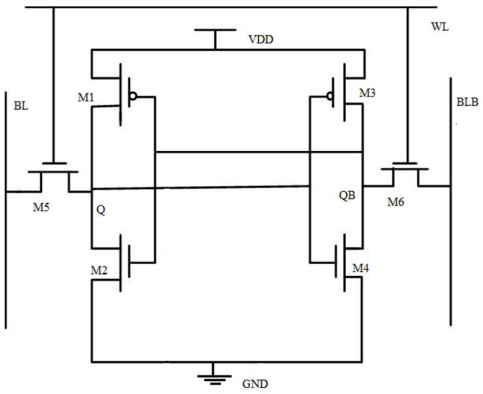

Figure 1. Conventional 6T SRAM

The paper is organized as follows. Section 2 describes related works. Section 3 gives the details of proposed work. Section 4 shows the result and its analysis. Section 5 concludes the paper.

II. Related Works

Due to the scaling in the CMOS technology, the leakage current increases the techniques for reducing the leakage current are acquiring more importance. Even though a high V_{th} CMOS can be considered as a solution to the mentioned problem, the operational speed of SRAM is affected. To increase the speed of operation and reduce the leakage of SRAM some design techniques are proposed.

A. Current mode sense amplification

As the technology scales down, the bit line capacitances are becoming too large for an SRAM circuit to drive. During the read operation, the output result is predetermined by the sense amplifier by sensing the differential current on the two-bit lines (BL1 and BLb1) as shown in Fig.2. By this method both the high speed and low power are feasible and but the delay is more at the output "Ref. [4-5]".

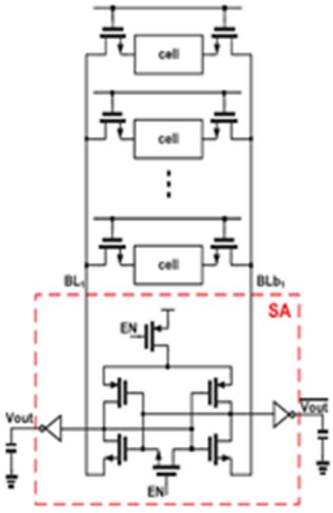

Figure 2. SRAM with sense amplification

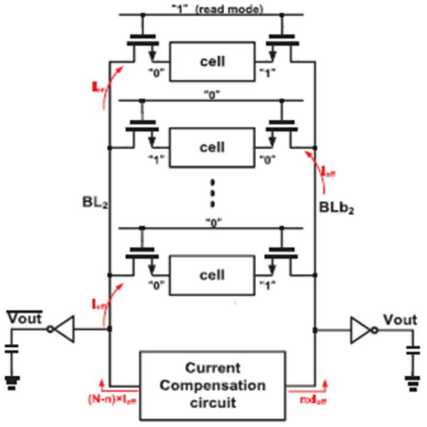

Figure 3. SRAM with current compensation technique

B. Current Compensation Technique

Fig.3 shows a current compensation circuit and in this case, the leakage current is detected by the compensation circuit when SRAM starts its operation and proper current is injected into the corresponding bit line "Ref. [6-7]". Consider the example of an array of SRAM having N cells in which n of the cells are stored with logic 1 and rest of the cells with logic 0. Whenever compensation circuit detects a bit line leakage, it injects $n \times I_{OFF}$ into BLb2, while $(N - n) \times I_{OFF}$ is injected into BL2, where I_{OFF} represents the cut-off leakage current. Once any of SRAM cell is activated in read mode, its speed is increased as its operation is not affected by the leakage of other cells. This method is used to increase the access speed but the leakage current of the SRAM is not reduced.

Another leakage current reduction technique is shown in Fig. 4. It contains a leakage current sensor and a compensation circuit. The voltage drop due to leakage current is sensed by the leakage current sensor and a compensation circuit is used to speed up the read operation of SRAM whenever a leakage is detected. Fig.5 shows the block diagram of the proposed system. The leakage current sensor part consists of an SRAM cell model followed by a comparator. SRAM cell model is used as a leakage monitor and generates a voltage proportional to the leakage current "Ref. [10]". A warning signal is produced whenever the v_leakage is more than the v_ref in order to activate the compensation circuit. Leakage in an SRAM cell is indicated by the increase in v_leakage. When v_leakage is higher than v_ref, the comparator produces a *low signal. As soon as a warning is produced, the transistor MP303 in compensation circuit is turned ON and it pulls up BLb such that BL drops fast as shown in Fig. 4. A positive feedback is used to speed up the read access.*

III. Proposed Work

The proposed circuit also contains a leakage current sensor and a compensation circuit as shown in Fig.3. The voltage drop due to leakage current is sensed by the leakage current sensor and a compensation circuit is used to speed up the read operation of SRAM whenever a leakage is detected and confirmed. The leakage current sensor part consists of an SRAM cell model followed by a comparator. SRAM cell model is used as a leakage monitor generating a voltage proportional to the leakage current "Ref. [17]". A warning signal is produced whenever the v_leakage is higher than v_ref in order to activate the compensation circuit. v_leakage rises to indicate that there is a leakage in the SRAM cell. When v_leakage is higher than v_ref, the comparator produces a low warning signal. As soon as a warning is produced, it is fed to the compensation circuit which consists of a transmission gate as shown in Fig.5.

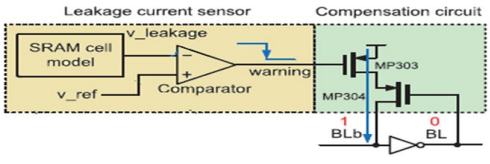

Figure 4. Block diagram of the system

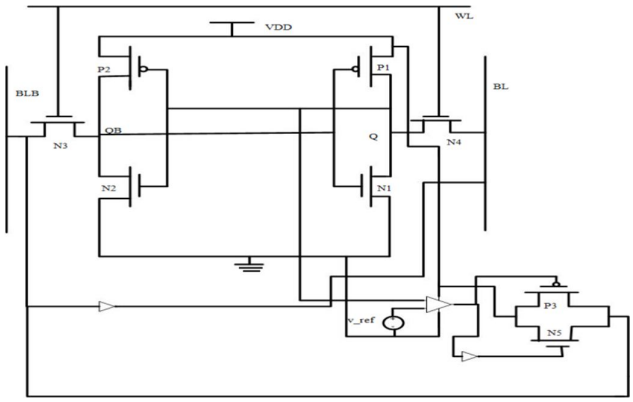

Figure 5. Schematic of complete circuit

A positive feedback is used to speed up the read access. As the bit line, BLB is initially precharged during the read operation, this compensation circuit operates only when bit 0 is accessed and it remains same while reading 1. As the bit line, BLB is initially precharged during the read operation, this compensation circuit operates only when bit 0 is accessed and it remains same while reading.

IV. Result and Discussion

Cadence Version IC 6.1.6. is used for simulation purpose and Virtuoso Schematic Editor is used for creating the schematic. The technology used was 180nm technology. The output of a comparator shown in Fig.7 clearly describes the operation of leakage sensing section. The reference voltage is set to 300mV and the output of the comparator is varied. When the leakage exceeds the reference voltage the comparator outputs a low signal which activates the compensation circuit which thereby produces a positive feedback to speed up read operation. The output of SRAM after compensation is shown in Figure 8. As Q changes from 0 to1 BL also change correspondingly.

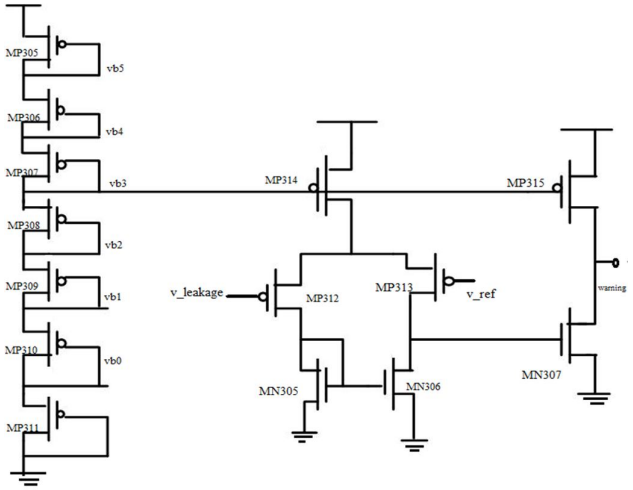

Figure 6. Schematic of a comparator

The power and delay obtained for the SRAM with compensation is shown in the Table1. Comparison of SRAM without compensation and with compensation is also given in the Table 1 and in Fig.9 and Fig.10 respectively. It is observed that read delay is reduced by 13% and power is reduced by 34% when compared to SRAM without compensation. As the read delay and power is reduced the proposed technique can be used as an effective to reduce the leakage power during the read operation of a SRAM and thus the performance of the SRAM can be increased.

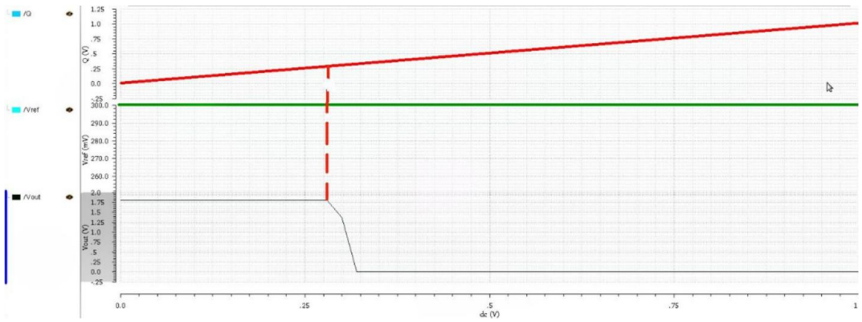

Figure 7. The output of a comparator

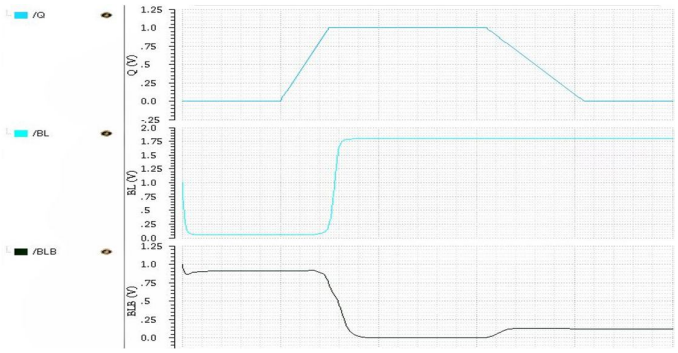

Figure 8. Output of SRAM with compensation

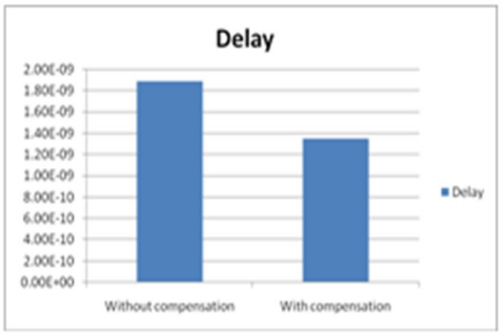

Figure 9. Comparison of delay

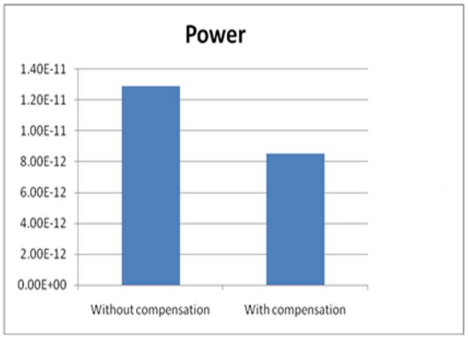

Figure 10. Comparison of power

TABLE I. DELAY AND POWER

	Without Compensation	With Compensation
Delay(s)	1.89E-09	1.65E-09
Power(W)	12.9E-12	8.50E-12

V. CONCLUSION

A read delay compensation design for 6T low supply voltage SRAM is presented in this paper. The proposed compensation design is composed of a leakage current sensor and a compensation circuit. A leakage current sensor consists of an SRAM cell model and a comparator. The leakage current sensor can sense the voltage drop caused by the leakage current. As soon as a warning signal issued by the leakage current sensor is over a predefined threshold, the compensation circuit which consists of a transmission gate speeds up the read

operation. By the measurement results, the read delay is reduced by 13% and power is reduced by 34% when compared to uncompensated SRAM.

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